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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,655	08/19/2003	Taiji Noda	740819-1027	3732

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/642,655	NODA, TAIJI	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Hideki JP patent No. 11040801.

Regarding claim 1 admitted prior art teaches (figs. 13A-13C and 14A and 14B) a method for manufacturing a semiconductor device, comprising: a first step of forming a gate (104) electrode on a semiconductor region via a gate insulator film (103); a step of implanting a first impurity (105A) of a first conductivity type (N) into the semiconductor region using the gate electrode (104) as a mask, having a certain depth; and a step of subjecting the semiconductor region to thermal annealing so as to form an extension high concentration diffusion layer (108) of the first conductivity type through diffusion of the first impurity, having a certain depth.

Admitted prior art does not teach, a second step of forming an amorphous layer in an upper portion of the semiconductor region by implanting ion of a group IV element into the semiconductor region using the gate electrode as a mask with an implantation projected range such that the first impurity reaches a position deeper than the amorphous layer and the extension high concentration diffusion layer having a junction at a position deeper than the amorphous layer.

Hideki teaches (figs. 1a-1c and 2a-2c) the formation of amorphous layer (13) using group IV element using the gate electrode (9) as mask, where the depth of layer (13) is shallower than regions (21) and (22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the amorphous layer taught by Hideki in the process of admitted prior art in order to restrain the acceleration of impurities.

The combined process of admitted prior art and Hideki would have the implantation range and the extension high concentration diffusion layer having a junction at a position deeper than the amorphous layer.

Regarding claim 2 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including the step of implanting a second impurity of a second conductivity type (P) into the semiconductor region using the gate electrode (104) as a mask with an implantation projected range such that the second impurity reaches a position deeper than the amorphous layer, and the fourth step includes a step of forming a pocket diffusion layer (106) of the second conductivity type (p) through diffusion of the second impurity under the extension high concentration diffusion layer (106A).

Regarding claim 3 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including a step of forming a side wall (107) made of an insulative film on a side surface of the gate electrode (104); and a step of implanting a third impurity of the first conductivity type (n) into the semiconductor region using the gate electrode and the side wall as a mask, and then performing thermal annealing, so as to form a high concentration diffusion layer (108) of the first conductivity type through diffusion of the third impurity, the high concentration diffusion layer of the first conductivity type being located on an outer side of the extension high concentration diffusion layer (106) and having a junction plane at a position deeper than the extension high concentration diffusion layer (fig. 14B admitted prior art).

Regarding claim 4 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including the group IV element is silicon or germanium (refer to section 25 of the machine translation of Hideki).

Regarding claim 5 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including implanting ion of the group IV element at a dose equal to or greater than a dose such that the semiconductor region is turned into an amorphous state. Since Hideki teaches layer (13) is amorphized, the applied dose is inherently equal to or greater than the dose that turns the semiconductor region to amorphous state.

Regarding claim 6 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above except explicitly stating that the third step includes implanting the second impurity with an implantation projected range of about 14 nm or less.

Parameters such as implantation depth and dose in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication process.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the implantation projected range of the combined process of admitted prior art and Hideki within the range as claimed in order to improve short channel effects.

Regarding claim 7 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including the second impurity is a molecule containing boron fluoride (page 2, 2nd paragraph of admitted prior art).

Regarding claim 8 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above except explicitly stating that the second impurity is boron.

Boron is a commonly used p-type impurity dopant that is widely known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute boron fluoride with boron in the process of admitted prior and Hideki in order to adjust the implantation depth.

Regarding claim 9 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claims 1 and 5 above including performing implantation of first impurity followed by thermal annealing to restore crystallinity of the semiconductor region.

Admitted prior art fails to teach performing a plurality of iterations of ion implantation and each of the iterations of ion implantation being followed by thermal annealing so as to restore a crystallinity of the semiconductor region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a plurality of iterations of ion implantation and each of the iterations of ion implantation being followed by thermal annealing in the process of admitted prior art in order to restrain the acceleration of impurities.

Regarding 10 the combined process admitted prior art and Hideki teaches substantially the entire claimed process of claim 1 above including a step of forming an insulating film (103) on the semiconductor region so as to cover an exposed portion of the semiconductor region.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SAG
April 29, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800